What is claimed is:

1. A frequency synthesiser according to a direct digital synthesis method comprising a phase accumulator for cyclical incrementation of a phase signal by a phase increment present at an input of the phase accumulator, with a memory unit containing a table of sine-function values stored in memory cells of the memory unit for determination of sine-function values corresponding to phase values of the phase signal, with a digital-to-analog converter for conversion of the time-discrete sine-function values into a quasi-analog sinusoidal time function and with an anti-aliasing low-pass filter for smoothing the quasi-analog sinusoidal time function, wherein

a non-periodic signal is superimposed over the time-discrete sinusoidal function values in an adder, which is connected between the memory unit and the digital-to-analog converter.

2. The frequency synthesiser according to claim 1, wherein the non-periodic signal is a noise signal.

3. The frequency synthesiser according to claim 2, wherein the non-periodic signal is a noise signal low-pass filtered in the low-frequency range.

4. The frequency synthesiser according to claim 1, wherein the phase accumulator, the memory unit, the adder and the digital-to-analog converter are synchronously timed with a common reference frequency.

5. The frequency synthesiser according to claim 4, wherein the noise signal bandpass-filtered in the low-frequency range is generated by a noise generator, which is controlled with a frequency-divided reference clock pulse obtained from a common reference clock pulse by an intermediate connection of a frequency divider.

6. The frequency synthesiser according to claim 5, wherein the frequency-divided reference clock pulse has a frequency which is reduced multiple times by comparison with the common reference clock pulse.

7. The frequency synthesiser according to claim 6, wherein the noise generator includes:

a pseudo-noise generator for generating a noise signal with a clock-pulse frequency which is reduced multiple times by comparison with the common reference clock pulse;

a first non-recursive filter for interpolating the noise signal generated by the pseudo-noise generator to a noise signal with a clock-pulse frequency which is reduced multiple times by comparison with the common reference signal;

a differentiator for filtering a direct component and low-frequency components out of the noise signal generated by the first non-recursive filter;

and

a second non-recursive filter for interpolating the noise signal generated by the differentiator to a noise signal with a clock-pulse frequency corresponding to the common reference frequency.

8. The frequency synthesiser according to claim 7, wherein the frequency of the frequency-divided reference clock pulse and the frequency limiting of the noise signal generated by the pseudo-noise generator are reduced four times by comparison with the common reference frequency, and the frequency limiting of the noise signal generated by the first non-recursive filter is reduced twice by comparison with the common reference frequency.

9. The frequency synthesiser according to claim 7, wherein the pseudo-noise generator includes two parallel-connected pseudo-noise generators, of which the outputs are interconnected via a combinatorial logic unit.

10. The frequency synthesiser according to claim 3, wherein the anti-aliasing low-pass filter is followed by an analog high-pass filter for suppression of the noise signal

bandpass-filtered in the low-frequency range in an output signal of the anti-aliasing low-pass filter.

11. The frequency synthesiser according to claim 10, wherein an output of the analog high-pass filter is supplied to a first input of a phase-locking loop.

12. The frequency synthesiser according to claim 11, wherein the phase-locking loop includes:

a phase detector for determining system deviation between an output frequency signal of the frequency synthesiser present at the output of the analog high-pass filter and a frequency-divided output frequency signal of the phase-locking loop;

a control filter for dynamic evaluation of the system deviation present at the output of the phase detector;

a voltage-controlled frequency oscillator for generating an output frequency signal dependent upon an output signal of the control filter; and

a mixer and a series-connected low-pass filter for coarse conversion of the output frequency signal by a value of a coarse-grid mixed-frequency signal present in the mixer.

13. The frequency synthesiser according to claim 12, wherein a frequency divider for frequency division of the output frequency signal coarsely converted by the mixer and a switching element, across which the frequency divider can be bridged via a direct connection, is connected downstream of the mixer.

14. The frequency synthesiser according to claim 12, wherein the coarse-grid mixed-frequency signal supplied to the mixer of the phase-locking loop is generated by a second phase-locking loop or by conversion from the common reference frequency.